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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/715,748	11/17/2000	Jean-Michel Reynes	SC0822ET	6966

7590

10/14/2003

Motorola Inc
Austin Intellectual Property Law Section
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EXAMINER

BERRY, RENEE R

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 10/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

RF

Office Action SummaryApplication No.
09/715,748Applicant(s)
Reynes et al.Examiner
Renee BerryArt Unit
2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ | 6) <input type="checkbox"/> Other: |

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent no. 6,091,114 to Mogul et al. in view of US patent no. 5,763,916 to Gonzalez et al.

In regard to claim 1, Mogul teaches a method of forming a diode for integration with a semiconductor device by providing a layer of semiconductor material; forming a dielectric layer over the layer of semiconductor material; introducing a first conductivity type dopant into the dielectric layer; forming a semi-conductive layer over the dielectric layer; introducing a second conductivity type dopant into a first region of the semi-conductive layer; the second region being adjacent the first region so as to provide a P/N junction of the diode at column 7, lines 40-53 to column 8, lines 1-5, claim 1.

In regard to claim 3, Mogul teaches the step of providing a layer of semiconductor material comprises the step of providing an epitaxial layer at column .

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In regard to claim 7, Mogul teaches the step of forming a semiconductive layer comprises the step of forming a layer of the one of the following material: polysilicon, and oxygen doped polycrystalline silicon (SIPOS)/polygate at column 6, lines 14-21 and column 8, lines 17-19.

In regard to claim 9, Mogul teaches a method of forming a transistor device having an integrated diode by providing a layer of semiconductor material; forming a first dielectric layer over the layer of semiconductor material having a first thickness; introducing a first conductivity type dopant into the first dielectric layer; patterning the first dielectric layer so as to provide an opening in the first dielectric layer extending to the layer of semiconductor material; forming a second dielectric layer over the layer of semiconductor material in the active area; forming a semi-conductive layer over the first and second dielectric layers; introducing a second conductivity type dopant into the semi-conductive layer; and semiconductive layer; introducing dopant of the first conductivity type; redistributing the first conductivity type dopant; and introducing a dopant of the second conductivity type into the regions of the first conductivity type at column 7, lines 40-53 to column 8, lines 1-5, claim 1.

However, Mogul does not teach all the limitations of the claims.

In regard to claims 1, 4, and 9 Gonzalez teaches forming a cap layer over the semi-conductive layer; forming first and second openings in the cap layer extending to the first and second regions of the semi-conductive layer; and forming contacts in the first and second openings to the first and second regions of the semi-conductive layer at column 5, lines 52-64.

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In regard to claim 6, Gonzalez teaches the cap layer comprises at least one dielectric layer at column 5, lines 52-65, reference number 54.

In regard to claim 8, Gonzalez teaches the step of introducing a second conductivity type dopant by forming a mask over the semiconductive layer; removing a portion of the mask so as to expose the first region of the semiconductive layer; and implanting the second conductivity type dopant into the first region of the semi-conductive layer at column 5, lines 14-24.

Therefore, it would have been obvious to one having ordinary skill in the art to have modified Mogul to include forming a cap layer over the semi-conductive layer; forming first and second openings in the cap layer extending to the first and second regions of the semi-conductive layer; and forming contacts in the first and second openings to the first and second regions of the semi-conductive layer; and introducing a second conductivity type dopant by forming a mask over the semiconductive layer; removing a portion of the mask so as to expose the first region of the semiconductive layer; and implanting the second conductivity type dopant into the first region of the semi-conductive layer, since such a modification would result in reduced leakage as described in column 1, lines 65-67 of Gonzalez et al.

Allowable Subject Matter

3. Claims 2 and 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 103, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

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Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. R. Berry whose telephone number is (703) 305-4544.



RRB

September 26, 2003



HOAI HO
PRIMARY EXAMINER